In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of transferring bursts of data between a processor device and a FIFO device, said transfer comprising:

triggering a burst transfer at the processor from ~~the~~ a change of state of a FIFO output signal by the FIFO device, said change of state being ~~the~~ an occurrence of a triggering event within the FIFO device; and

inhibiting the FIFO device from changing state of the FIFO output signal thereby inhibiting of triggering of any further burst transfers until a current burst transfer is complete.

2. (Original) The method of claim 1, wherein:

said triggering event is change in a FIFO fullness indicator flag.

3. (Original) The method of claim 2, wherein:

said FIFO fullness indicator flag denotes the FIFO is less than or greater than half full; and

said triggering event is changing from said FIFO fullness indicator flag denoting less than half full to greater than half full.

4. (Original) The method of claim 2, wherein:

said fullness indicator denotes less than or greater than half full; and

said triggering event is changing from said FIFO fullness indicator flag denoting greater than half full to less than half full.

5. (Original) The method of claim 1, wherein:

said burst transfer includes transfer of predetermined amount of data in fixed number of sequential clock cycles.

6 to 8. (Cancelled)

9. (Currently Amended) The method of claim 1, ~~further comprising the step of~~ wherein:

said step of inhibiting the FIFO device from changing state of the FIFO output signal, thereby inhibiting further burst transfers includes further inhibiting the FIFO device from changing state of the FIFO output signal until a predetermined number of clock cycles following completion of current burst transfer.

10. (New) The method of claim 1, wherein:

said step of inhibiting the FIFO device from changing state of the FIFO output signal, thereby inhibiting further burst transfers includes

the processor device supplying to the FIFO device an end of burst signal upon completion of a burst transfer, and

inhibiting the FIFO device from changing state of the FIFO output signal until receipt of said end of burst signal.

11. (New) The method of claim 1, wherein:

said step of inhibiting the FIFO device from changing state of the FIFO output signal, thereby inhibiting further burst transfers includes

the FIFO device counting a predetermined number of cycles corresponding to a burst transfer size, and

inhibiting the FIFO device from changing state of the FIFO output signal until completion of counting the predetermined number of cycles.